REMARKS

Applicants are amending the claims of the above-identified application, prior to examination thereof, in order to further clarify the definition of the present invention, in light of, for example, the references applied by the Examiner in the Office Action mailed May 30, 2003, in prior Application No. 10/138,485, filed May 6, 2002, of which the above-identified application is a Continuation application filed under 37 CFR § 1.53(b).

Specifically, the undersigned respectfully directs attention to claim 24 of the present application, corresponding to claim 25 of No. 10/138,485, claim 25 having been allowed in No. 10/138,485. Claim 24 has not been amended, as compared to claim 25 of No. 10/138,485; and it is respectfully submitted that claim 24 should be allowed in the present application.

The remaining claims as originally filed in the above-identified application, claims 1-23, correspond respectively to claims 1-9 and 11-24 of No. 10/138,485. Of original claims 1-23 in the above-identified application, the subject matter of claim 12 has been incorporated into claim 11; and, correspondingly, claim 12 has been cancelled without prejudice or disclaimer. In view of canceling of claim 12, dependencies of claims 13 and 16 have been amended. In addition, claim 17 has been amended to recite that an elastic modulus of the adhesive film, in a range of mounting reflow temperature for mounting a semiconductor element having the adhesive film onto a mounting substrate, is more than 1 MPa. Furthermore, all of claims 1-11 and 13-23 have been amended to recite that the method or structure is

adapted to be used in ball grid array semiconductor devices. Note, for example, the paragraph bridging pages 1 and 2 of Applicants' specification.

In addition, Applicants are adding new claims 25-33 to the application. Claim 25, dependent on claim 24, recites that the adhesive layer is adapted to be used in ball grid array semiconductor devices. Claims 26, 28, 30 and 32, dependent respectively on claims 1, 11, 17 and 19, recite that the claimed structure includes pads for electrical connection thereto by a ball grid array connection. Claims 27, 29, 31 and 33, dependent respectively on claims 1, 11, 17 and 19, recite that the elastic modulus of the adhesive layer is at most 2000 MPa in a range of -55°C to 150°C. Note, for example, the paragraph bridging pages 15 and 16 of Applicants' specification.

Applicants respectfully note the references applied by the Examiner in rejecting claims in the Office Action mailed May 30, 2003, in prior Application No. 10/138,485, that is, Japanese Patent Document No. 6-236906, International (PCT) Published Application No. WO 93/05582 (WO '582), and the article by Nakayoshi, et al., "Memory Package with LOC Structure Using New Adhesive Material", in 1994 IEEE (1994), pages 575-579, and respectfully submit that all of the present claims patentably distinguish over the teachings of these references under the requirements of 35 USC §103.

It is respectfully submitted that these applied references do not disclose, nor would have suggested, a circuit tape, or adhesive film, or method of manufacturing circuit tape, having an adhesive layer, and adapted to be used in ball grid array semiconductor devices, as in all of the present claims (other than claim 24), wherein an elastic modulus of the adhesive layer, in a range of mounting reflow temperature

for mounting a semiconductor element onto a mounting substrate, is more than 1 MPa. Note each of claims 1, 11, 17 and 19.

Furthermore, it is respectfully submitted that these applied references would have neither taught nor would have suggested such circuit tape with an adhesive layer, or such adhesive film, or such method of manufacturing circuit tape with an adhesive layer, adapted to be used in ball grid array semiconductor devices, as in the present claims, having the recited elastic modulus, and wherein the circuit tape includes pads for electrical connecting a semiconductor element thereto by a ball grid array connection. See claims 26, 28, 30 and 32.

Moreover, these references would have neither disclosed nor would have suggested such circuit tape, or such adhesive film, or such method, as in the present claims, wherein the elastic modulus of the adhesive film, in a range of 250°C-200°C, is more than 1 MPa (see, e.g., claims 2, 13 and 20); and/or wherein the elastic modulus of the adhesive layer at room temperature is lower than the elastic modulus of the adhesive layer in a temperature range of 200°C-250°C (see claim 7); and/or wherein an elastic modulus of the adhesive film at room temperature is equal to or less than 4000 MPa (note claims 6, 16 and 21); and/or wherein the elastic modulus of the adhesive layer is at most 2000 MPa in a range of -55°C - 150°C (note claims 27, 29, 31 and 33).

In addition, it is respectfully submitted that the teachings of these references applied in No. 10/138,458 would have neither disclosed nor would have suggested such a circuit tape, or such adhesive film, or such method, as in the present claims, having a three-layer structure having a porous support layer and two adhesive layers which are respectively applied onto both sides of the porous support layer (see

claims 4, 14 and 22); and/or wherein the adhesive film includes structure wherein an adhesive agent is impregnated into a porous support (see claims 5, 15 and 23); and/or wherein the adhesive layer includes the layer of a thermoplastic resin, with the thermoplastic resin having a glass transition temperature greater than 250°C (see claim 8). As will be explained in detail later, the article by Nakayoshi, et al., is directed to providing a single-layer adhesive tape, teaching away from the layered structure, or use of a porous support, as in various of the present claims.

Furthermore, it is respectfully submitted that the teachings of the references applied in No. 10/138,458 would have neither disclosed nor would have suggested such circuit tape, or such adhesive film, or such method of manufacturing a circuit tape with an adhesive layer, as in the present claims, including the features set forth in the independent claims, as discussed previously, and having additional features as in the remaining claims in the application, including (but not limited to) wherein the adhesive layer has a layer with a thermoplastic resin, the thermoplastic resin having a glass transition temperature greater than 250°C (see claim 8); and/or wherein the material of the adhesive layer has a coefficient of moisture absorption at 85°C/85% RH for 168 hours of, at most 3% (see claim 9); and/or wherein the circuit tape has an uneven surface between portions of the circuit, with the adhesive layer filling in these spaces (see claim 10); and/or wherein the method includes punching out adhesive film of a size smaller than that of the elongated circuit tape and adhering continuously the punched-out adhesive film to the circuit tape, as the circuit tape is transferred from a first reel to a second reel, concurrently with the punching (note claim 17), particularly wherein the punched-out adhesive film is punched out

from an elongated adhesive film transferred from a first reel to a second reel (see claim 18).

All of the present claims, except claim 24, are directed to an adhesive film, a circuit tape with an adhesive layer, or a method for manufacturing circuit tape with an adhesive layer, adapted to be used in ball grid array semiconductor devices (note, in particular, claims 26, 28, 30 and 32, reciting that the circuit tape includes pads for electrical connection thereto by a ball grid array connection). Such ball grid array structure has a shortened connecting terminal length, which makes fast signal transmission possible; and also has an increased width of the conductor, so that this structure is also effective in decreasing inductance. However, since organic materials used generally in such ball grid array structurehave a larger thermal expansion coefficient than the semiconductor element, and such ball grid array structures generally require relatively high temperatures for connection, to which the element and organic materials are exposed, thermal stress generated by the difference in thermal expansion becomes a problem from the point of view of connection reliability.

In view of this problem, recently there has been proposed a structure which does not use a carrier substrate for the ball grid array package. The proposed package structure uses a circuit tape composed of a polyimide and the like, instead of a carrier substrate, for electrically connecting the semiconductor element and the mounting substrate. Electrical connections between the semiconductor element and the circuit tape are provided by a wire bonding method or a bonding connection with leads, and the circuit tape and the mounting substrate are electrically connected by soldering ball terminals.

An elastomeric material has been used as a stress buffer layer. As the elastomeric material used, a silicone material is generally used, since this is a material having a low modulus of elasticity and a superior heat resistance; and, as a general method for forming a stress buffer layer with the silicone material, an uncured liquid resin is printed on the circuit tape using masks, and subsequently the printed resin is cured. However, this technique of providing the stress buffer layer including use of the uncured liquid resin has problems, such as a difficulty in maintaining the flatness of the stress buffer layer obtained by the printing, and the complexity of the printing process.

Against this background, Applicants provide a method, and formed structure, having a stress buffer layer which is superior in flatness, thereby obtaining semiconductor devices which are superior in mass productivity. Applicants have found that by using, as an adhesive layer on the circuit tape, adapted to be used in ball grid array semiconductor devices, an adhesive layer having an elastic modulus of more than 1 MPa in a range of mounting reflow temperature for mounting the semiconductor element onto a mounting substrate, objectives according to the present invention are achieved; and, in particular, a stress buffer layer that is generally flat, and can be easily used, even if used at the relatively high reflow temperatures in forming ball grid array connections, can be achieved.

For example, according to the present invention, by using an adhesive material having a high elastic modulus in the range of the reflow temperature, particularly where such material has a relatively low moisture absorption rate, a foaming phenomenon can be avoided. During the relatively high temperature heat treatment of solder reflow for mounting a semiconductor element onto a mounting

substrate, moisture evaporates, and the film material swells due to vapor pressure of the moisture. When the swelling exceeds a threshold value, a foaming phenomenon is generated, and defects, such as void formation, delamination and the like, are generated. Through use of adhesive materials having an elastic modulus, in the temperature range of the reflow process, of at least 1 MPa, especially where such material has a relatively low moisture absorption rate, such foaming can be avoided, so that the adhesive material has superior characteristics during reflow operations. Note the paragraph bridging pages 4 and 5 of Applicants' specification.

In addition, Applicants have found that when materials, of which the elastic modulus in the temperature range of the mounting reflow condition is maintained at least at 1 MPa, are used, a preferable result in the anti-reflow characteristics can be obtained. By using a material having a high elastic modulus in the range of the reflow temperature, in providing the ball grid array connection structure, the reflow characteristics can be improved as to both the swelling amount and mechanical characteristics. Note the paragraph bridging pages 5 and 6 of Applicants' specification.

In addition, as described in the paragraph bridging pages 36 and 37 of Applicants' specification, the film material is superior in flatness, so that a manufacturing method which is superior in workability can be provided; and in view of the stress buffering effect achieved by the film according to the present invention, the connection reliability of both the lead portion which electrically connects the circuit tape and the semiconductor element, and the bump which electrically connects the semiconductor device and the mounting substrate, can be satisfied simultaneously in a temperature cycling test.

WO '582 discloses assemblies incorporating semiconductor chips which include a semiconductor chip having a front surface with a plurality of contacts disposed in a pattern on the front surface. The chip assembly includes a sheetlike dielectric element, referred to in this patent document as an "interposer", overlying the front surface of the chip, the interposer having a first surface facing toward the chip and a second surface facing away from the chip. An area of the interposer overlies the contact pattern area of the chip, and the interposer has apertures extending through it from the first surface to the second surface, and also has a plurality of electrically conductive terminals disposed in a pattern on the second surface of the interposer. See page 7, lines 20-37 of this patent document. This patent document also discloses that the assembly includes flexible, electrically conductive leads which preferably extend through the apertures in the interposer, each such lead having a contact end connected to the associated contact of the chip and a terminal end connected to the associated terminal on the second surface of the interposer. See page 8, lines 5-11. This patent document further discloses that the assembly may also include a compliant dielectric encapsulant having a low elastic modulus, such as an elastomeric encapsulant, covering the flexible leads in whole or in part. See page 9, lines 5-8. Note also, for example, page 19, lines 1-17, of this patent document. This patent document further discloses that the adhesive layer 302 (note Figs. 10A-10B) may be omitted where the conductive layer forms a satisfactory bond to the material of the interposer.

In the paragraph bridging pages 32 and 33 of WO '582, together with, for example, Fig. 13, is shown an assembly method according to one embodiment described therein, having a sheet-like dielectric interposer 836 assembled to

chip 820, interposer 836 including a flexible top layer 838 formed by a thin sheet of material having a relatively high elastic modulus and a compliant bottom layer 840 formed from a material having a relatively low elastic modulus. An alternate, generally similar arrangement includes an interposer incorporating a flexible top layer similar to the top layer 838 of the interposer as discussed above. In this arrangement this interposer may also include a separate compliant underlayer disposed between the top layer and the chip front surface, and also disposed beneath terminals, i.e., between the terminals and the chip. Note the paragraph bridging pages 41 and 42 of WO '582.

It is respectfully submitted that WO '582 is concerned with providing a compliant interposer between the chip and terminals, to permit independent movement of the individual terminals during application of test probes. It is respectfully submitted that this patent document does not disclose, nor would have suggested, an adhesive layer as in the present invention, having an elastic modulus of more than 1 MPa, much less advantages achieved thereby in use in ball grid array semiconductor devices.

It is respectfully submitted that the other references applied by the Examiner against claimed subject matter in the Office Action mailed May 30, 2003 in No. 10/138,485, would not have rectified the deficiencies of WO '582 in connection with the presently claimed subject matter, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Nakayoshi, et al. discloses a single-layer thermoplastic polyimide siloxane adhesive tape used for lead-on-chip structure. This article discloses that due to absence of a base film, the single-layer adhesive can be fabricated to any desired

thickness; and by providing large Young's modulus of film at high temperature and by providing a contamination-free lead surface, a sufficient lead-wire bondability can be achieved. Note the Abstract on page 575 of this article. Note also the left-hand column on page 578, disclosing an evaluation of bondability on the inner leads by different Young's modulus level of thermoplastic adhesive tape at wire bond temperatures; and the description that the author has found that the adhesive which keeps high Young's modulus during the wire bond process (that is, has high glass transition temperature) does not cause the deformation of inner leads. This portion of the article goes on to disclose that to obtain the bondability in view of the result of the simulation and evaluation, the author has selected an adhesive (adhesive B, shown in Table 1 on page 576) which has Young's modulus higher than 1×10^9 Pa at wire bond temperature.

It is emphasized that Nakayoshi, et al. is directed to lead-on-chip structure, not ball grid array structure. It is respectfully submitted that one of ordinary skill in the art concerned with ball grid array structure would not have looked to the teachings of Nakayoshi, et al. In this regard, it is respectfully submitted that in a package having a lead-on-chip structure as in Nakayoshi, et al., bonding by reflowing the solder is not necessary; and, accordingly, it is respectfully submitted that issues arising in connection with ball grid array connection structure, including, e.g., evaporation of moisture at the solder reflow step, does not occur in connection with lead-on-chip structure. Accordingly, it is respectfully submitted that Nakayoshi, et al. provides no information relevant to the technical issues involved with respect to providing ball grid array structure, as discussed previously; and it is respectfully submitted that one of ordinary skill in the art would not have looked to

the teachings of Nakayoshi, et al., in connection with solder reflow as used in ball grid array techniques, absent hindsight use of Applicants' disclosure, which of course is improper under 35 USC §103.

In any event, even if one of ordinary skill in the art would have looked to the disclosure of Nakayoshi, et al., in connection with ball grid array structure as in the present claims, it is respectfully submitted that the disclosure thereof, even in combination with the teachings of WO '582, would have neither disclosed nor would have suggested elastic modulus of the adhesive layer, providing advantages as in the present invention; and, moreover, would have taught away from the multiple layer structure for the adhesive film as in various of the present claims, emphasizing that Nakayoshi, et al. is directed to single-layer thermoplastic polyamide siloxanes.

Japanese Patent Document No. 6-236906 discloses an adhesive tape for a semiconductor, provided on the insulating film, with the adhesive tape having an adhesive layer 2 and a protective layer 3, and in which the Young's modulus after hardening at 20°C - 300°C of the adhesive layer is 4×10^8 dyne/cm^2 or greater. This patent document discloses that such tape provides for transfer mold mounting or the wire bonding mounting of a tape for TAB, by preventing conversion or deterioration at high temperature of an adhesive.

Even assuming, arguendo, that the teachings of the Japanese Patent Document were properly combinable with the teachings of WP '582 and of Nakayoshi, et al., it is respectfully submitted that the combined teachings of the references would have neither disclosed nor would have suggested use of an adhesive layer having the recited elastic modulus in ball grid array semiconductor devices, and advantages thereof, achieved by the present invention.

That is, it is respectfully submitted that the present invention realizes particular advantages preventing generation of defects such as foaming with attendant blistering, void generation and peeling off of film material in the mounting reflow step; and that avoidance of such foaming phenomenon, through use of an adhesive layer, in ball grid array semiconductor devices, having an elastic modulus of more than 1 Mpa, would have neither been disclosed nor would have been suggested by the teachings of the applied references.

In view of the foregoing, examination of the above-identified application, including in light of prior art cited and applied in prior Application No. 10/138,485; and allowance of all claims presently in the application, are respectfully requested.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees and excess claim fees, to Deposit Account No. 01-2135 (referencing case No. 503.35443CC4) and please credit any excess fees to such deposit account.

Respectfully submitted,

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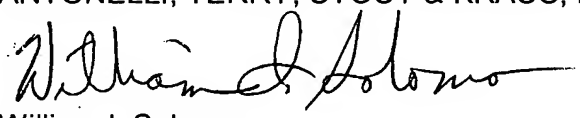

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